PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Furukawa et al. Art Unit: 2814
Serial No.: 10/767,039 Examiner: Phat X. Cao
Filed: January 29, 2004 Atty. Docket No.: ROC920030272US1
For: VERTICAL FIELD EFFECT TRANSISTORS INCORPORATING SEMICONDUCTING NANOTUBES GROWN IN A SPACER-DEFINED PASSAGE

Cincinnati, Ohio 45202 Date: March 27, 2006

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

DECLARATION UNDER RULE 131

We, Toshiharu Furukawa, Mark Charles Hakey, Steven John Holmes, David Vaclav Horak, Peter H. Mitchell, and Larry Alan Nesbit (the inventors), being duly cautioned and sworn, submit this Declaration in response to the Office Action dated February 9, 2006, and state:

That we are the inventors of the invention entitled "VERTICAL FIELD EFFECT TRANSISTORS INCORPORATING SEMICONDUCTING NANOTUBES GROWN IN A SPACER-DEFINED PASSAGE" described and claimed in the application for Letters Patent of the United States, Serial No. 10/767,039, filed January 29, 2004 ('039 application);

That this is a Declaration under the provisions of Rule 131 and the rules of practice for the United States Patent Office in support of said '039 application;

That the invention described and claimed in the '039 application was conceived prior to September 25, 2003, the publication date of U.S. Patent Application Publication No. 2004/0178617 in the name of Appenzeller et al.;

That, as evidence of the conception of the invention described and claimed in the '039 application, attached and incorporated into this Declaration as Exhibit A are copies of original annotated drawings bearing a date (now masked) made by one or all of the undersigned inventors prior to September 25, 2003 and bearing a date before September 25, 2003 (but with said date now masked);

That the attached Exhibit includes a detailed description of a vertical semiconductor

device structure, which clearly demonstrates that such vertical semiconductor device structure embodies the elements claimed in at least the independent claims of the '039 application, and which was conceived prior to the publication date of Appenzeller et al.;

That the conception of the invention claimed in at least pending independent claims 1, 42, and 47 of the '039 application is fully supported by the attached Exhibit, and that all annotated drawings and text included in the Exhibit having been created in the United States by one or all of the undersigned inventors before September 25, 2003;

That the Exhibit demonstrates as follows:

That a semiconductor device structure was conceived before September 25, 2003;

That the semiconductor device structure included a substrate defining a substantially horizontal plane; a gate electrode projecting vertically from said substrate and including a vertical sidewall; a spacer of a dielectric material flanking said vertical sidewall and spaced horizontally from said vertical sidewall of said gate electrode to define a vertical passage, said spacer extending vertically relative to said gate electrode such that said passage has a vertical dimension greater than or equal to a vertical height of said vertical sidewall of said gate electrode; a semiconducting nanotube positioned in said vertical passage and extending between opposite first and second ends with a substantially vertical orientation; a gate dielectric disposed on said vertical sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube;

That the semiconductor device structure may have alternatively included a substrate; a gate electrode projecting from said substrate and including a sidewall; a first spacer of a dielectric material flanking said sidewall to define a passage; a semiconducting nanotube positioned in said passage between said sidewall and said spacer and extending between opposite first and second ends, said semiconducting nanotube having a length such that said second end of said semiconducting nanotube projects above said gate electrode; a gate dielectric disposed on said sidewall between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source;

That the semiconductor device structure may have alternatively included a gate electrode projecting from said substrate and including a sidewall; a first spacer of a dielectric

material flanking said sidewall of said gate electrode to define a passage; a semiconducting nanotube positioned in said passage between said sidewall of said gate electrode and said spacer, said semiconducting nanotube extending between opposite first and second ends; a gate dielectric disposed on said sidewall of said gate electrode between said semiconducting nanotube and said gate electrode; a source electrically coupled with said first end of said semiconducting nanotube; and a drain electrically coupled with said second end of said semiconducting nanotube, said gate electrode being positioned between said drain and said source;

as called for in the pending independent claims in the '039 application;

That the undersigned inventors were diligent from prior to the publication date of September 25, 2003, which represents the publication date of U.S. Patent Application Publication No. 2004/0178617, to January 29, 2004, which represents the filing date of the '039 application. Specifically, the undersigned inventors can account for the entire period during which reasonable diligence is required with affirmative acts and acceptable excuses. During this period, the attorneys acted with reasonable diligence on the application. Specifically, in-house counsel for the Assignee was diligent in reviewing the attached Exhibit prepared by the inventors and forwarding the attached Exhibit to outside counsel for the Assignee on July 15, 2003. Outside counsel for the Assignee was diligent in drafting a specification the '039 application and forwarding a draft specification to the inventors on October 21, 2003. In particular, outside counsel for the Assignee had a reasonable backlog of unrelated cases taken up in chronological order and carried out expeditiously. The inventors were diligent in reviewing and approving the draft specification between October 21, 2003 and November 4, 2003. Outside counsel for the Assignee was diligent in finalizing the specification of the '039 application, after receiving comments from the inventors' review, and forwarding the finalized specification to in-house counsel for the Assignee on November 4, 2003. In-house counsel for the Assignee was diligent in forwarding the specification for the '039 application and a Declaration/Power of Attorney to the inventors and, subsequently, filing the '039 application and the executed Declaration/Power of Attorney at the U.S. Patent and Trademark Office on January 29, 2004;

Therefore, in summary, the Declaration and attached Exhibit constitute a showing of facts, in character and weight, that establish conception of the invention prior to the publication date of U.S. Patent Application Publication No. 2004/0178617 for a semiconductor device structure that

is the subject of and is claimed in Application Serial No. 10/767,039, all the acts of which occurred in the United States BEFORE September 25, 2003, and thus precede the publication date of U.S. Patent Application Publication No. 2004/0178617, and that the inventors and counsel for the inventors exhibited diligence from prior to the publication date of September 25, 2003 to the filing date of the '039 application.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Further declarants sayeth naught.

By _____
Toshiharu Furukawa

Date _____

By _____
Mark Charles Hakey

Date _____

By _____
Steven John Holmes

Date _____

By _____
David Vaclav Horak

Date _____

By _____
Peter H. Mitchell

Date _____

By Larry Allen Nesbit
Larry Alan Nesbit

Date March 30, 2006

Li Melander 3/30/2006
My Commission Expires Feb. 10, 2007

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Further declarants sayeth naught.

By _____
Toshiharu Furukawa

Date _____

By _____
Mark Charles Hakey

Date _____

By _____
Steven John Holmes

Date _____

By _____
David Vaclav Horak

Date _____

By Peter H. Mitchell
Peter H. Mitchell

Date March 30 2006

By _____
Larry Alan Nesbit

Date _____

STATE OF VERMONT
CHITTENDEN COUNTY, SS

At Jericho, this 30 day of MARCH A.D. 2006
personally appeared PETER H. MITCHELL
and acknowledged this instrument, by him sealed
and subscribed, to be his free act and deed.
Before me, Jessica L Alexander Notary Public

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Further declarants sayeth naught.

By _____
Toshiharu Furukawa

Date 3/30/2006

By _____
Mark Charles Hakey

Date _____

By _____
Steven John Holmes

Date 3/30/2006

By _____
David Vaclav Hora

Date 3/30/06

By _____
Peter H. Mitchell

Date _____

By _____
Larry Alan Nesbit

Date _____

Denise M. Swiss
Notary Public, State of New York
County of Greene
Reg. No. 01SW6084940
Commission Expires Dec. 18, 2006

_____

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Further declarants sayeth naught.

By _____
Toshiharu Furukawa

Date _____

By Mark Charles Hakey
Mark Charles Hakey

Date 3/31/2006

By _____
Steven John Holmes

Date _____

By _____
David Vaclav Horak

Date _____

By _____
Peter H. Mitchell

Date _____

By _____
Larry Alan Nesbit

Date _____